★ 100% EAS Guaranteed
★ Green Device Available
★ Super Low Gate Charge
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

Product Summary

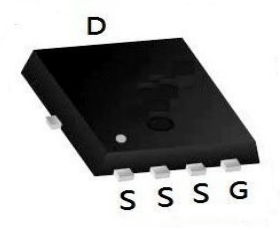
BVDSS	RDSON	ID
65V	3.5mΩ	100A

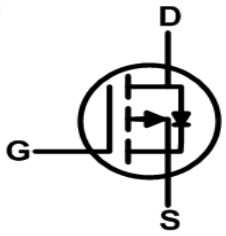
Description

The XXWS100N06LF is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The XXWS100N06LF meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PRPAK5X6 Pin Configuration





Absolute Maximum Ratings (T_A = 25°C, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	65	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	100	A
	T_C=100°C		61	
Pulsed Drain Current[1]		I_{DM}	380	A
Single Pulse Avalanche Energy[2]		EAS	80	mJ
Total Power Dissipation	T_C=25°C	P_D	73.5	W
Operating Junction and Storage Temperature Range		T_J , T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	51	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.7	°C/W

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	65	-	-	V
Gate-body Leakage Current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = 65V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.7	2.5	V
Drain-Source On-Resistance[4]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	3.5	4.8	mΩ
			V_{GS} = 4.5V, I_D = 10A	-	4.8	6.6	
Forward Transconductance[4]		g_{fs}	V_{DS} = 10V, I_D = 20A	-	89	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = 30V, V_{GS} =0V, f =1MHz	-	2180	-	pF
Output Capacitance		C_{oss}		-	735	-	
Reverse Transfer Capacitance		C_{rss}		-	42	-	
Gate Resistance		R_g	f = 1MHz	-	1.8	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 30V, I_D= 20A	-	35	-	nC
Gate-Source Charge		Q_{gs}		-	6.6	-	
Gate-Drain Charge		Q_{gd}		-	8.4	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DD} = 30V, R_G = 3Ω, I_D= 20A	-	9.4	-	ns
Rise Time		t_r		-	8.4	-	
Turn-Off Delay Time		$t_{d(off)}$		-	32.5	-	
Fall Time		t_f		-	12.5	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F=20A, dI/dt=100A/μs	-	50	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	20	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	100	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C
2. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH，I_{AS}=40A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

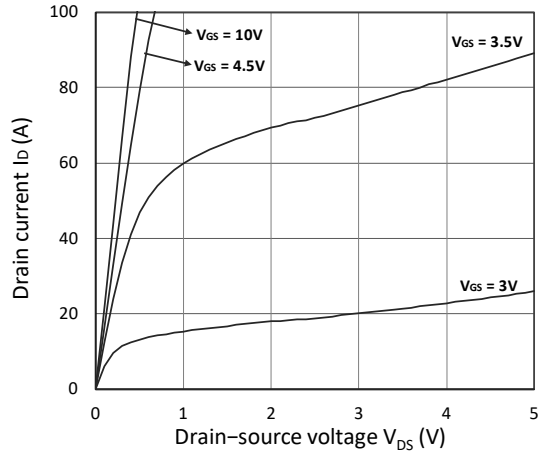


Figure 1. Output Characteristics

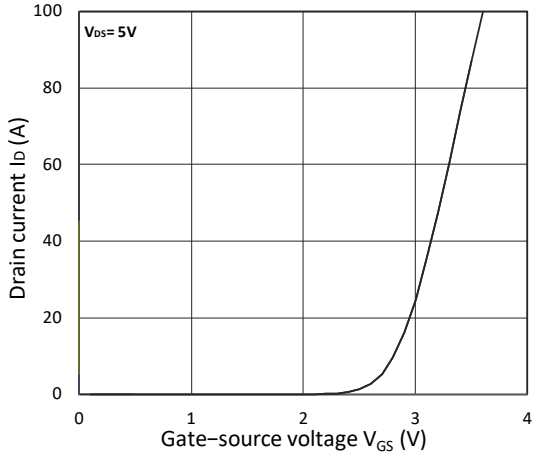


Figure 2. Transfer Characteristics

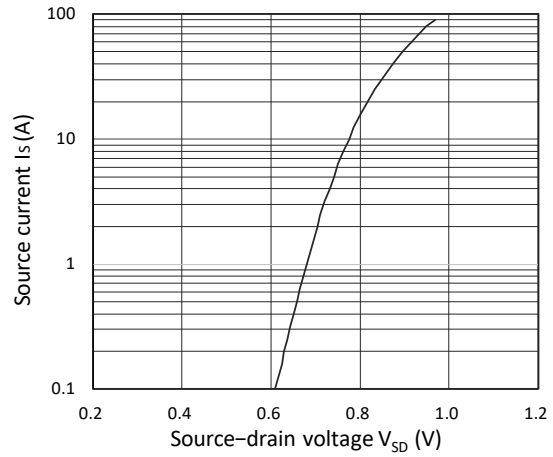


Figure 3. Forward Characteristics of Reverse

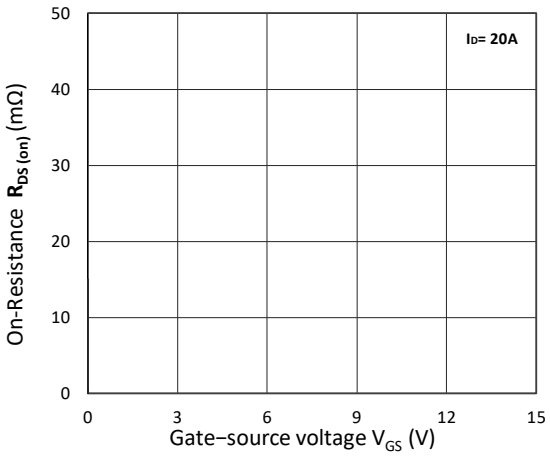


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

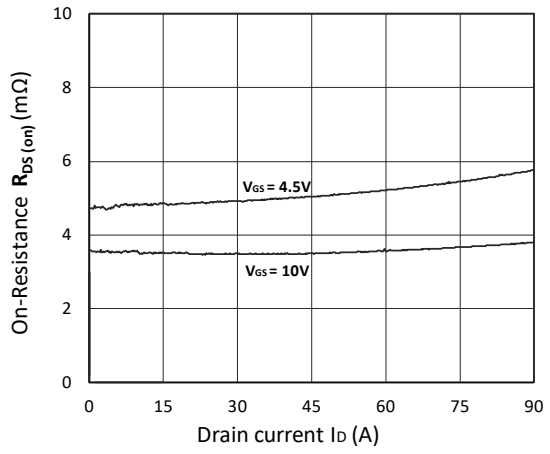


Figure 5. $R_{DS(ON)}$ vs. I_D

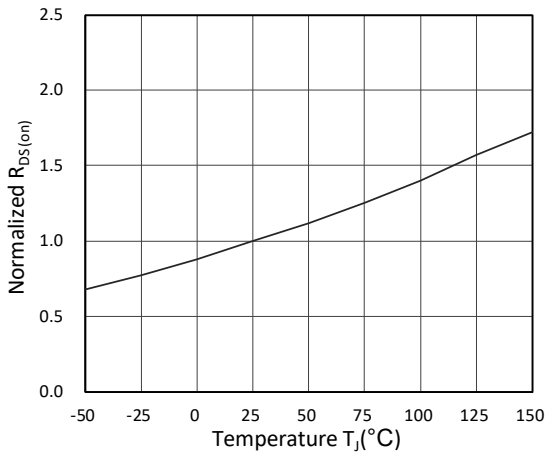


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

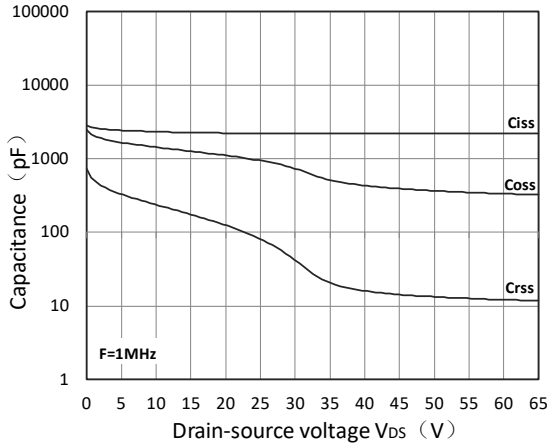


Figure 7. Capacitance Characteristics

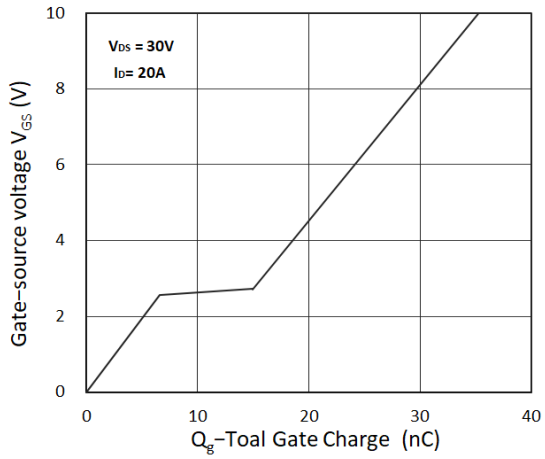


Figure 8. Gate Charge Characteristics

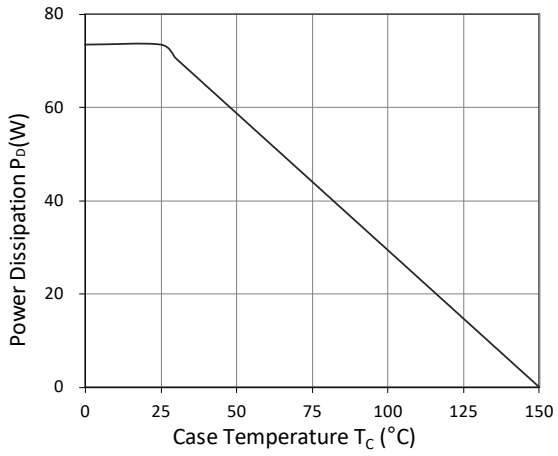


Figure 9. Power Dissipation

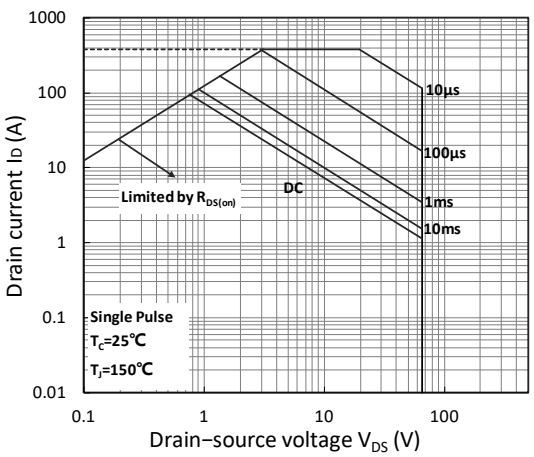


Figure10. Safe Operating Area

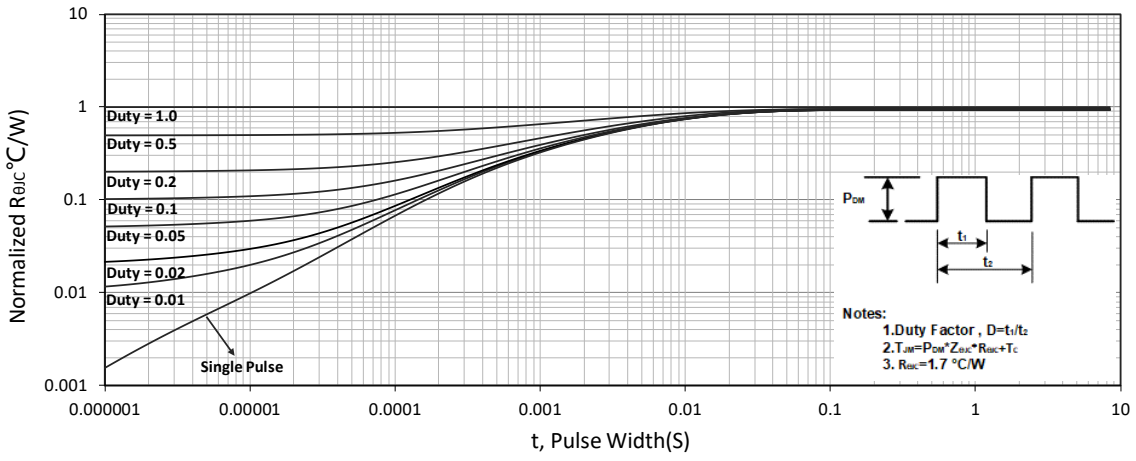


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

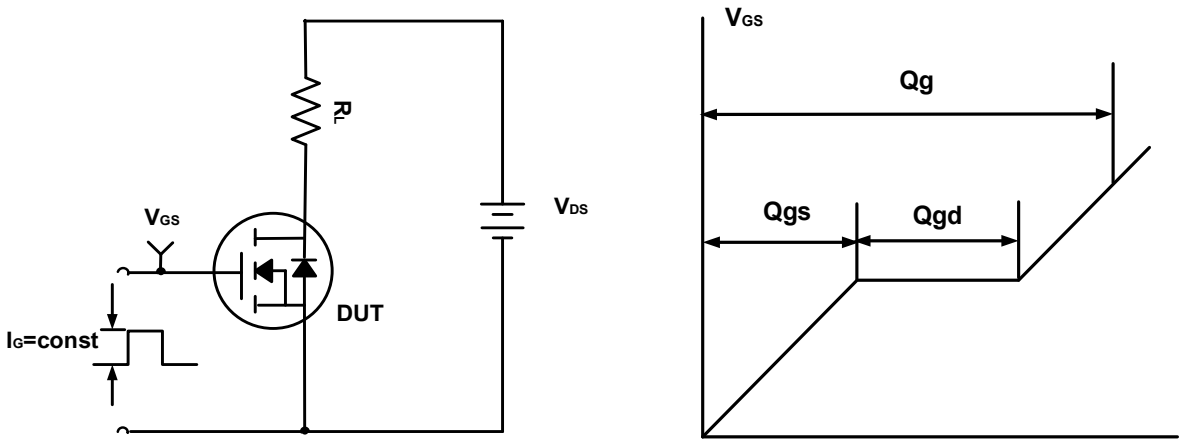


Figure A. Gate Charge Test Circuit & Waveforms

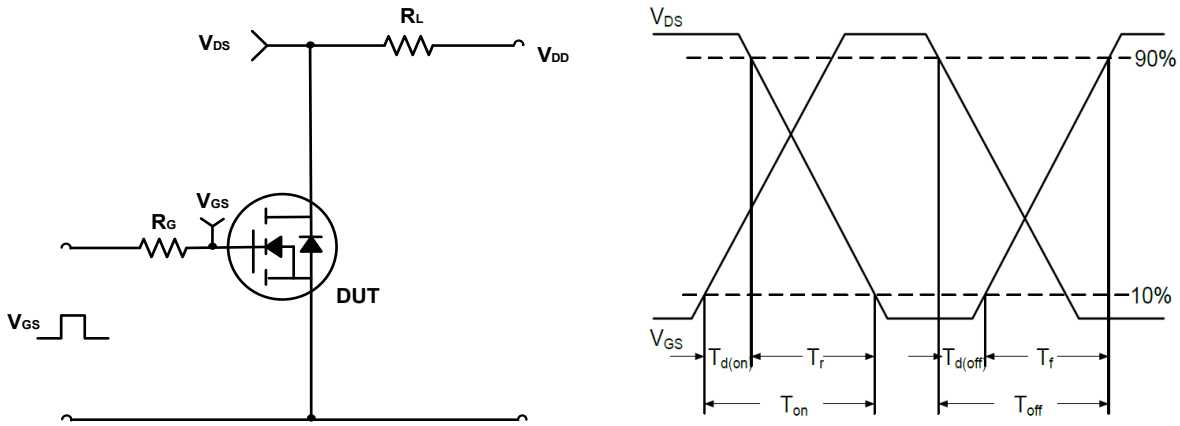


Figure B. Switching Test Circuit & Waveforms

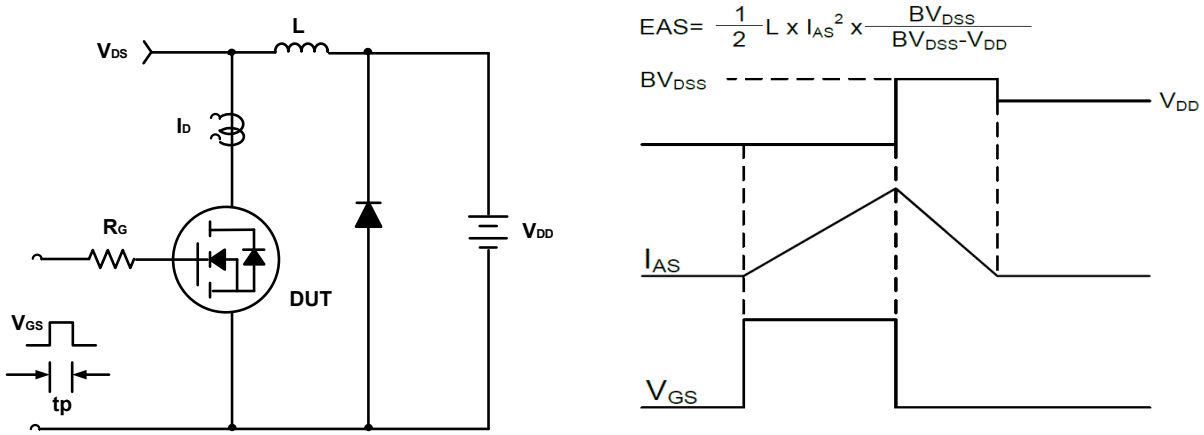
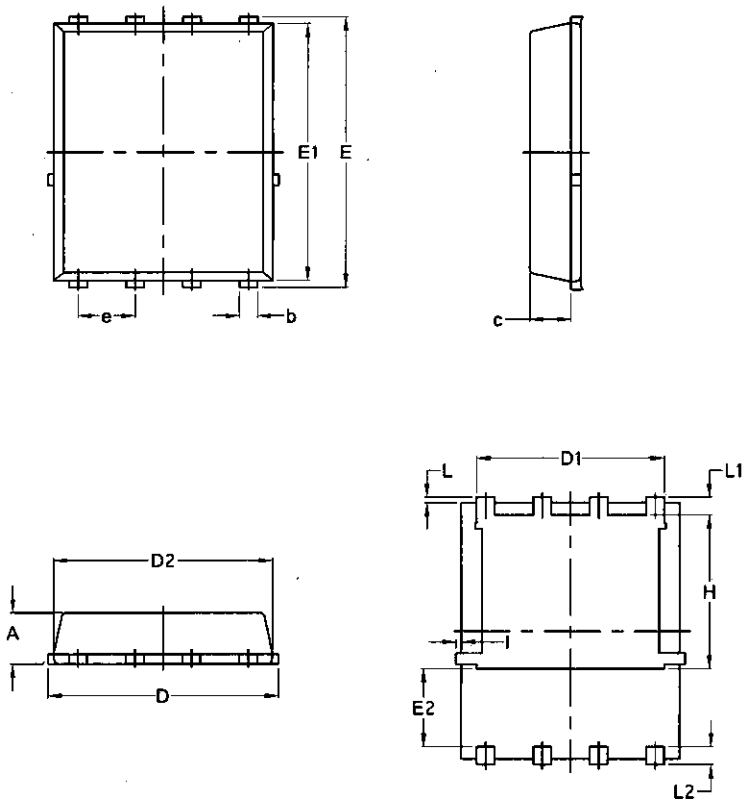


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070