



### Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

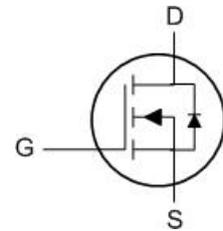
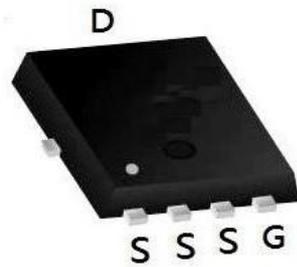
### Product Summary

BVDSS	RDSON	ID
30V	3.8mΩ	65A

### Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

### PDFN5060-8L Pin Configuration



### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	±20	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	65
		$T_C=100^\circ\text{C}$	41
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	260	A
Single Pulse Avalanche Energy <sup>2</sup>	$E_{AS}$	20	mJ
Total Power Dissipation	$P_D$	31.25	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$	60	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	4	°C/W

**Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise noted)**

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>							
Drain-Source Breakdown Voltage		<b>V<sub>(BR)DSS</sub></b>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30	-	-	V
Gate-body Leakage Current		<b>I<sub>GSS</sub></b>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T <sub>J</sub> =25°C	<b>I<sub>DSS</sub></b>	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V	-	-	1	μA
	T <sub>J</sub> =100°C			-	-	100	
Gate-Threshold Voltage		<b>V<sub>GS(th)</sub></b>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.6	2.4	V
Drain-Source On-Resistance <sup>4</sup>		<b>R<sub>DS(on)</sub></b>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	3.8	5	mΩ
			V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	-	6	8	
Forward Transconductance <sup>4</sup>		<b>g<sub>fs</sub></b>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A	-	130	-	S
<b>Dynamic Characteristics<sup>5</sup></b>							
Input Capacitance		<b>C<sub>iss</sub></b>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1MHz	-	905	-	pF
Output Capacitance		<b>C<sub>oss</sub></b>		-	475	-	
Reverse Transfer Capacitance		<b>C<sub>rss</sub></b>		-	57	-	
Gate Resistance		<b>R<sub>g</sub></b>	f = 1MHz	-	1.9	-	Ω
<b>Switching Characteristics<sup>5</sup></b>							
Total Gate Charge		<b>Q<sub>g</sub></b>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 20A	-	16	-	nC
Gate-Source Charge		<b>Q<sub>gs</sub></b>		-	3	-	
Gate-Drain Charge		<b>Q<sub>gd</sub></b>		-	3.3	-	
Turn-On Delay Time		<b>t<sub>d(on)</sub></b>	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 15V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	6.3	-	ns
Rise Time		<b>t<sub>r</sub></b>		-	3.2	-	
Turn-Off Delay Time		<b>t<sub>d(off)</sub></b>		-	18	-	
Fall Time		<b>t<sub>f</sub></b>		-	3.6	-	
Body Diode Reverse Recovery Time		<b>t<sub>rr</sub></b>	I <sub>F</sub> = 20A, dI/dt = 100A/μs	-	10	-	ns
Body Diode Reverse Recovery Charge		<b>Q<sub>rr</sub></b>		-	13.2	-	nC
<b>Drain-Source Body Diode Characteristics</b>							
Diode Forward Voltage <sup>4</sup>		<b>V<sub>SD</sub></b>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V
Continuous Source Current		<b>I<sub>S</sub></b>	T <sub>C</sub> = 25°C	-	-	65	A

**Notes:**

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C.
2. The EAS data shows Max. rating . The test condition is V<sub>DD</sub> = 25V, V<sub>GS</sub> = 10V, L = 0.1mH, I<sub>AS</sub> = 20A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

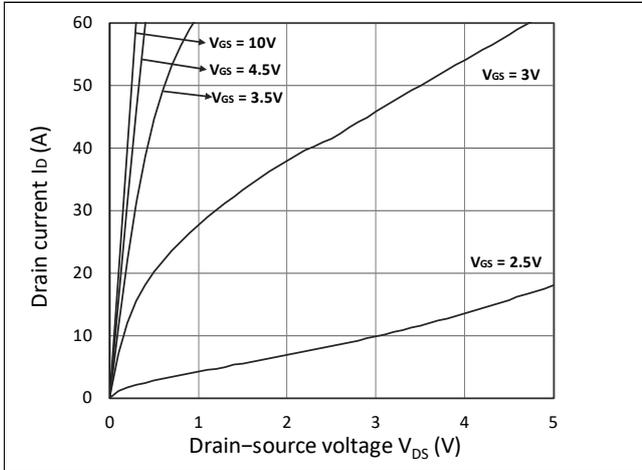
**Typical Characteristics**


Figure 1. Output Characteristics

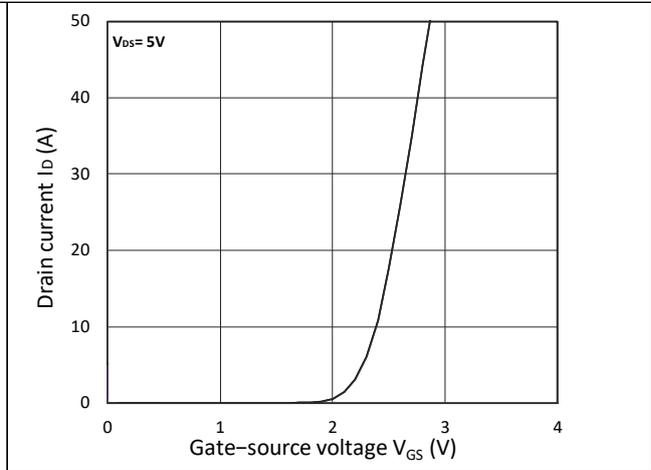


Figure 2. Transfer Characteristics

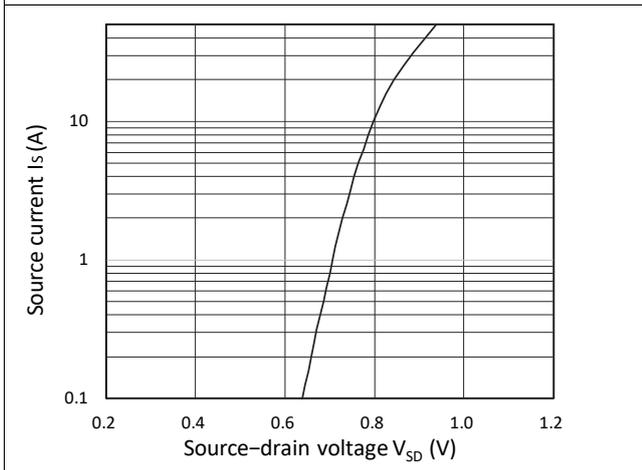
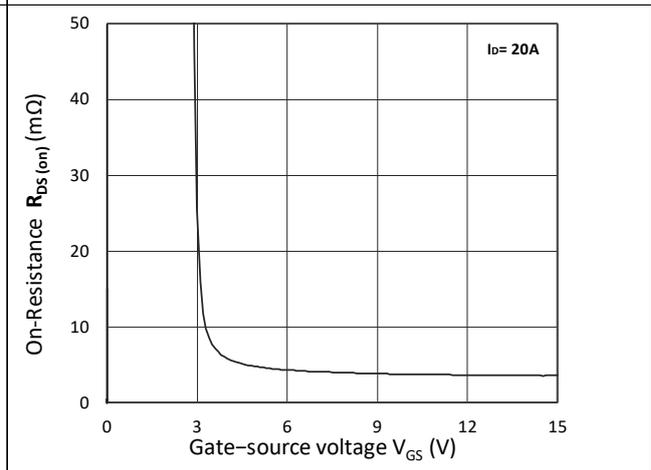
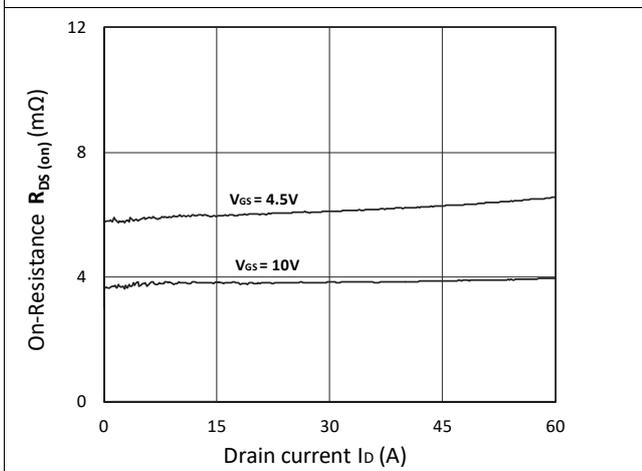
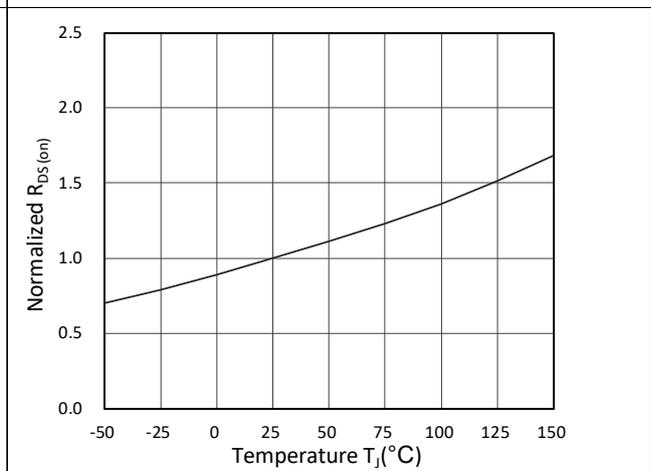


Figure 3. Forward Characteristics of Reverse


 Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$ 

 Figure 5.  $R_{DS(ON)}$  vs.  $I_D$ 

 Figure 6. Normalized  $R_{DS(ON)}$  vs. Temperature

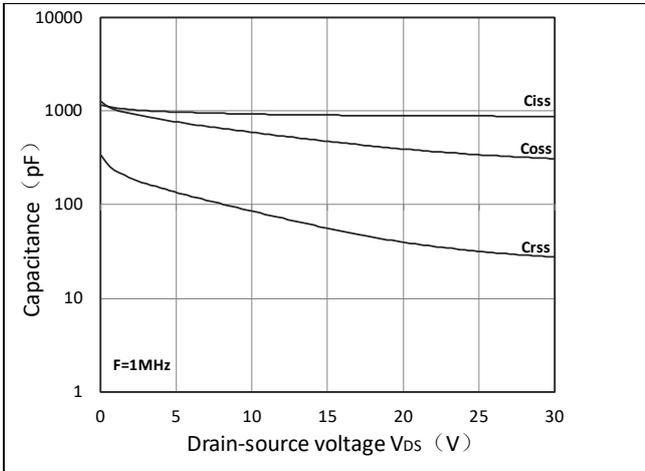


Figure 7. Capacitance Characteristics

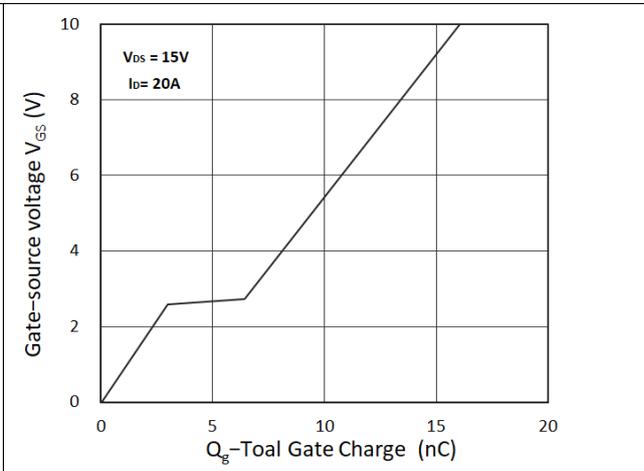


Figure 8. Gate Charge Characteristics

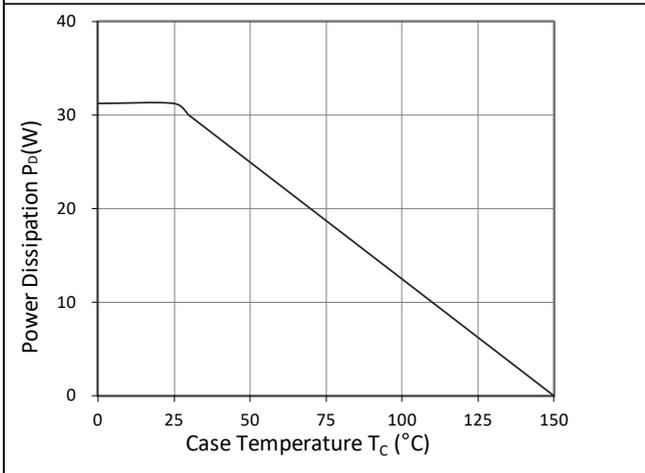


Figure 9. Power Dissipation

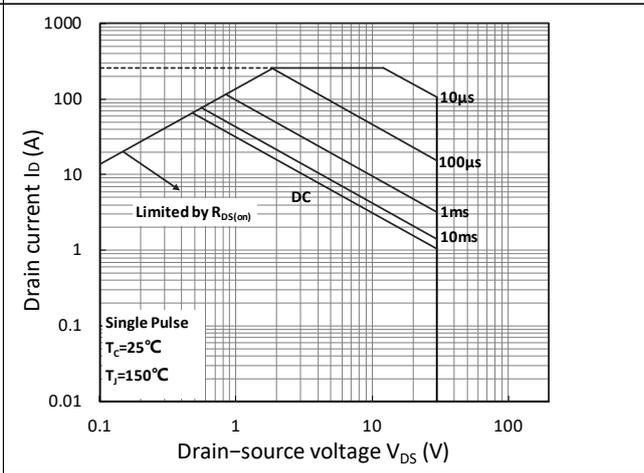


Figure 10. Safe Operating Area

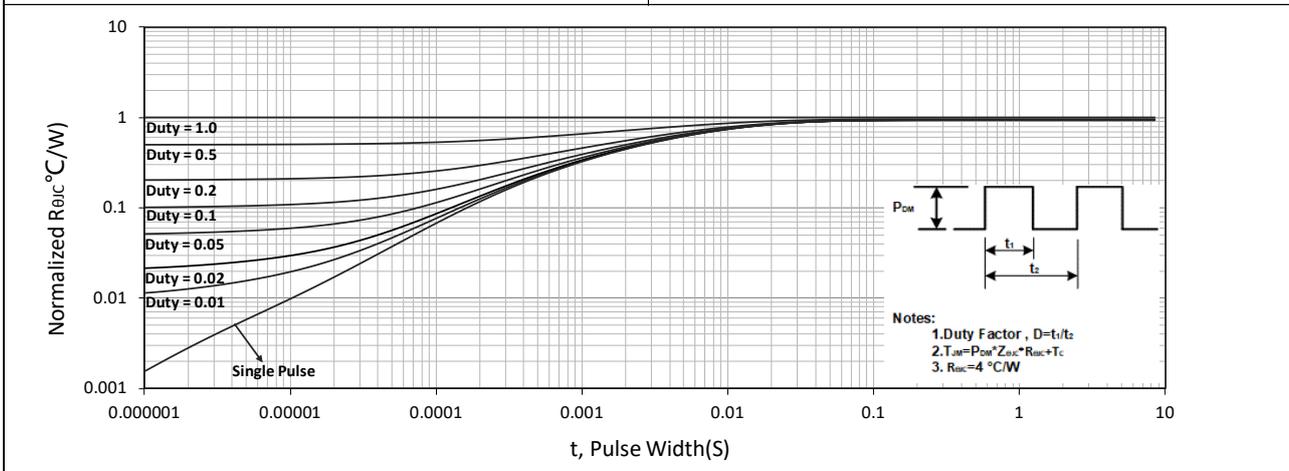


Figure 11. Normalized Maximum Transient Thermal Impedance

### Test Circuit

DFN5X6-8L Package Information

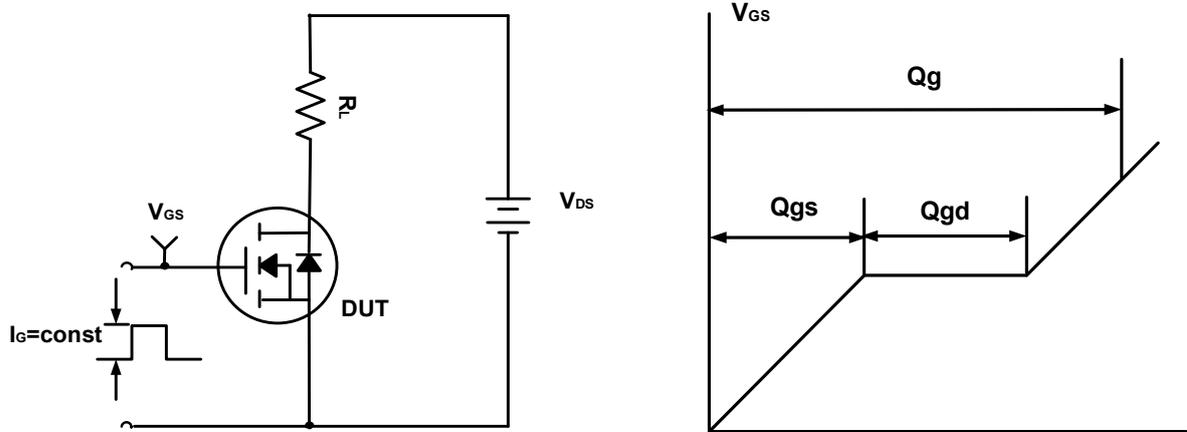


Figure A. Gate Charge Test Circuit & Waveforms

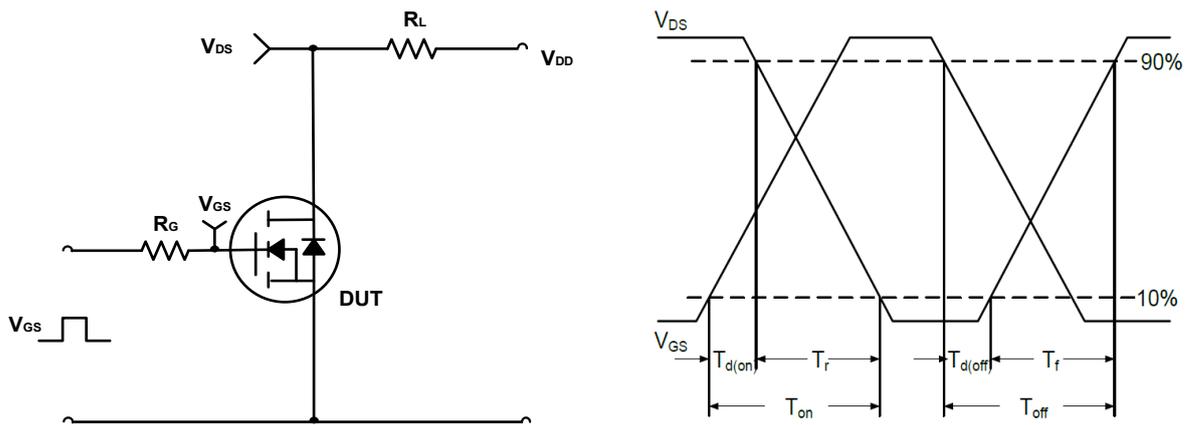


Figure B. Switching Test Circuit & Waveforms

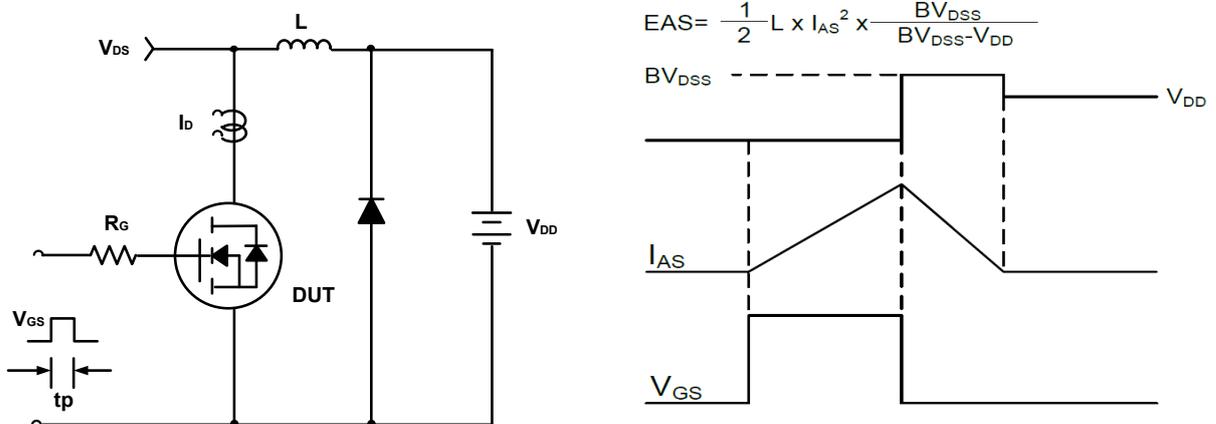
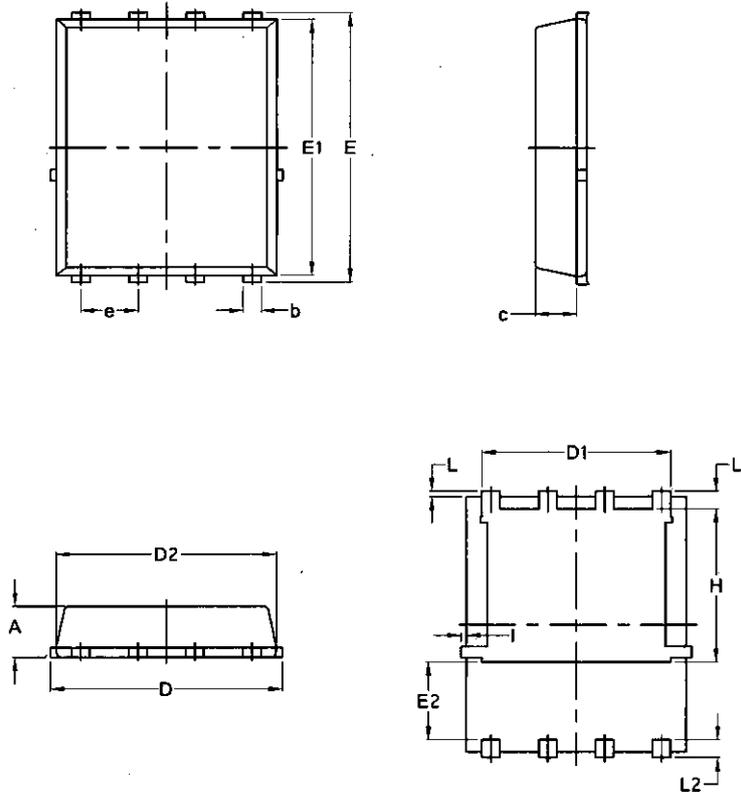


Figure C. Unclamped Inductive Switching Circuit & Waveforms

**Package Mechanical Data-PDFN5060-8L- Single**


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070